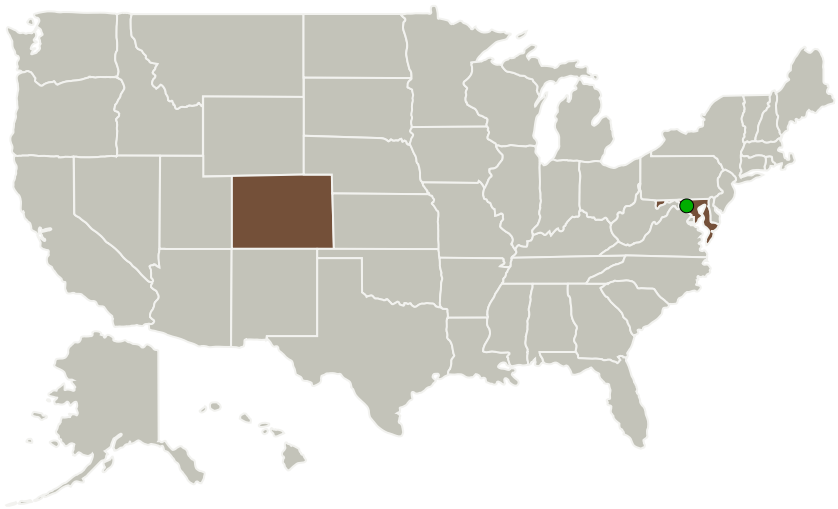
Radiation Hardened Structured ASIC Platform for Rapid Chip Development for Very High Speed System on a Chip (SoC) and Complex Digital Logic Systems, Phase I

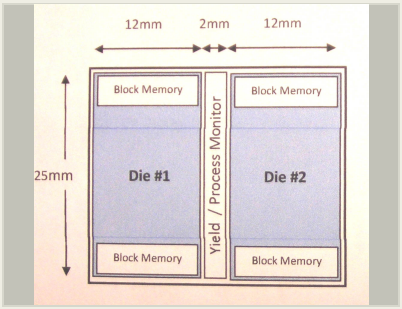
Completed Technology Project (2014 - 2014)

Project Introduction

Radiation Hardened Application Specific Integrated Circuits (ASICs) provide for the highest performance, lowest power and size for Space Missions. In order to dramatically reduce the development cycle and reduce the cost to tapeout Rad Hard ASICs, we propose a Structured ASIC approach. In this approach we fix an array of complex logic cells and provide a fixed Area Array for I/O pads supporting in excess of 400 CMOS GPIO pins. In addition, we fix the power grid and the pins associated with power (core and I/O) and ground. Thus, we require only routing in a subset of the metal layers in order to configure the Structured ASIC to a specific design. This leads to substantial reduction in design and verification time to tapeout, and results in reduced cost by requiring a subset of Mask changes per design. In this work, we will build on existing 90nm Silicon proven Radiation Hardened Structured ASIC platform and develop a Structured ASIC platform at the 45nm SOI technology node with the objective to increase the clock speeds to hundreds of MHz with SEU mitigation in sequential logic. We will also use High Density Interconnect (HDI) for packaging the Die in BGA and LGA packages. The HDI design does not change for each configuration of the Structured ASIC so that the same benefits of Structured ASIC are extended to packaging the part with high pinout and high speed I/O requirements eliminating layout design costs.

Primary U.S. Work Locations and Key Partners





Radiation Hardened Structured ASIC Platform for Rapid Chip Development for Very High Speed System on a Chip (SoC) and Complex Digital Logic Systems Project Image

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Organizations Performing Work	Role	Type	Location
Microelectronics Research Development Corporation	Lead Organization	Industry	Colorado Springs, Colorado
Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations	
Colorado	Maryland

Project Transitions

June 2014: Project Start

December 2014: Closed out

Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/140589)*

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Microelectronics Research Development Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:

Sasan Ardalan

Co-Investigator:

Sasan Ardalan

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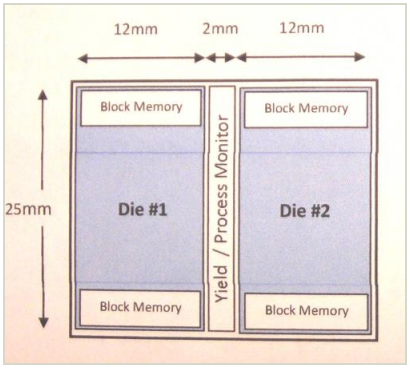
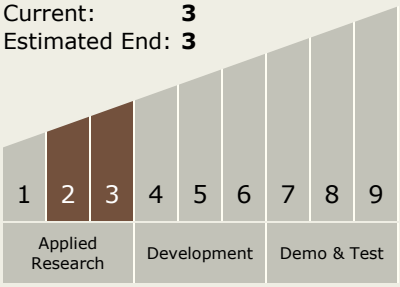
Images



Project Image
Radiation Hardened Structured ASIC Platform for Rapid Chip Development for Very High Speed System on a Chip (SoC) and Complex Digital Logic Systems Project Image
(https://techport.nasa.gov/image/126172)

Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **3**



Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.6 Radiation Hardened ASIC Technologies

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System